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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,922	08/27/2003	Kiran V. Chatty	BUR920030045US1	1921

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,922	CHATTY ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9 and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata (6,469,354) in view of White et al. (5,589,423).

Regarding claims 2 and 11, Hirata teaches in figure 1B and 3A and related text a latch-up robust ESD integrated circuit comprising: one or more I/0 cells each having one or more I/0 pads 22 wherein no n-diffusions are directly connected to the one or more I/O pads, and

wherein each of said one or more I/0 pads is coupled to an associated and distinct one or more silicide blocked p-type field effect transistors 32 having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide, and wherein said gate is positioned between a p-diffusion of said source 16p and drain 14p,

a n-diffusion 18p is connected to said gate and said p-diffusion of said source 16p;

said transistor is coupled to an I/0 pad 22 that is connected to said p-diffusion of said drain 16p, and the I/O pad has no connection to n-diffusion of said transistor.

Regarding the claimed limitations of a transistor having a snapback voltage that is less than the breakdown voltage of said gate oxide, these features are inherent in Hirata's device, because Hirata's structure is identical to the claimed structure.

Figure 1B does not depict an n-diffusion 18p is directly connected to said gate and said p-diffusion of said source 16p of transistor 31 and is spaced apart from said p-diffusion of said source. Hirata teaches in figure 3A a p-diffusion 18n is directly connected to said gate and said p-diffusion of said source 16n of transistor 32 and is spaced apart from said n-diffusion of said source. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form transistor 31 as transistor 32 is formed, such that an n-diffusion 18p is directly connected to said gate and said p-diffusion of said source 16p of transistor 31 and is spaced apart from said p-diffusion of said source, in order to simplify the processing steps of making the device by making the device as taught by Hirata.

Regarding the claimed limitation of a silicide blocked p-type field effect transistor, Hirata teaches an ESD device that does not comprise silicide. Therefore, forming the device using a silicide blocked p-type field effect transistor is a process limitation which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. Therefore, Hirata's structure is at least obvious over the claimed structure.

In the alternative, White et al. forms a silicide blocked p-type field effect transistor by using a silicide blocked layer (see abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a silicide blocked p-type field effect transistor in Hirata's device in order to prevent silicidation of protective devices.

Regarding claims 3 and 12, Hirata teaches said source is coupled to a voltage and said gate is coupled to said source and said drain is coupled said I/0 pad.

Regarding claims 4-5 and 13-14, Hirata teaches in figures 1B and 3A a body terminal coupled to the source of the transistor.

Regarding claims 6 and 15, Hirata does not teach a snapback voltage of at most 5 volts. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a snapback voltage of at most 5 volts in Hirata's device in

order to use the device in an application which requires a snapback voltage of at most 5 volts.

Regarding claims 7-8 and 16-17, Hirata teaches in figure 3A a p-type resistor coupled to said transistor and coupled said I/0 pad.

Regarding claims 9 and 18, Hirata does not teach a diffusion resistor. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a diffusion resistor in Hirata's device in order to have better control over the properties of the resistor.

Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata and White et al., as applied to claims 2, 7, 11 and 16 above, and further in view of Applicant Admitted Prior Art (AAPA).

Hirata and White et al. teach substantially the entire claimed structure, as applied to claims 2, 7, 11 and 16 above, except forming the resistor between said transistor and said I/0 pad. AAPA teaches in figure 1 forming a resistor between the protection device and the I/0 pad. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's resistor between said transistor and said I/0 pad, so that a first voltage appearing at said I/0 pad is of a different magnitude than a second voltage appearing at said transistor, said first and second voltages

differing by a value proportional to the resistance of said p-type resistor in Hirata and White et al.'s device, in order to improve the protection capability of the device.

Response to Arguments

Applicant argues that Hirada teaches in figure 3A an n-type transistor 31 and not a p-type transistor, and therefore all the required elements, as recited by claims 2 and 11, are not taught by Hirada.

The examiner agrees that Hirada teaches in figure 3A an n-type transistor 31, and not a p-type transistor. However, the rejection states that Hirada teaches in figure 1B and related text a p-type transistor 32, which has all the elements, as required by claims 2 and 11.

The rejection further states that Figure 1B does not depict an n-diffusion 18p is directly connected to said gate and said p-diffusion of said source 16p of transistor 31 and is spaced apart from said p-diffusion of said source. That is, figure 1B does not depict the connections of transistor 32. However, Hirata teaches in figure 3A the connections of the n-type transistor 31, wherein a p-diffusion 18n is directly connected to said gate and said p-diffusion of said source 16n of transistor 32 and is spaced apart from said n-diffusion of said source.

Applicant argues that Hirada does not teach I/0 pads wherein no n-diffusions are directly connected to the one or more I/O pads.

Hirada teaches in figure 3A and related text I/0 pads 22 connected only to an n-diffusion 14n wherein no p-diffusions are directly connected to the one or more I/O pads. However, since figure 3A depicts an n-type transistor, and the rejection is based on a p-type transistor 32 (as shown in figure 1B), the I/0 pads 22 of transistor 32 are connected only to a p-diffusion, and thus no n-diffusions are directly connected to the one or more I/O pads 22 (of transistor 32), as claimed.

Conclusion

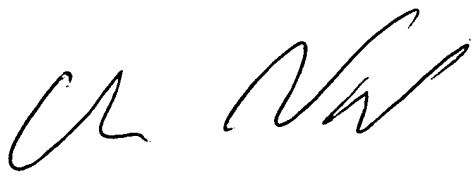
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
4/29/06

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